High-Mobility Strained-Si PMOSFET's

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Abstract—**Operation and fabrication of a new high channel-mobility strained-Si PMOSFET are presented. The growth of high-quality strained Si layer on completely relaxed, step-graded, SiGe buffer layer is demonstrated by gas source MBE. The strained-Si layer is characterized by double crystal X-ray diffraction, photoluminescence, and transmission electron microscopy. The operation of a PMOSFET is shown by device simulation and experiment. The high-mobility strained-Si PMOSFET is fabricated on strained-Si, which is grown epitaxially on a completely relaxed step-graded $Si_{0.82}Ge_{0.18}$ buffer layer on Si(100) substrate. At high vertical fields (high $|V_g|$), the channel mobility of the strained-Si device is found to be 40% and 200% higher at 300 K and 77 K, respectively, compared to those of the bulk Si device. In the case of the strained-Si device, degradation of channel mobility due to Si/SiO_2 interface scattering is found to be more pronounced compared to that of the bulk Si device. Carrier confinement at the type-II strained-Si/SiGe-buffer interface is clearly demonstrated from device transconductance and C-V measurements at 300 K and 77 K.**

I. Introduction

THE speed of very large scale integrated (VLSI) circuits has been improving steadily due to the aggressive scaling of device dimensions. As dimensions shrink to the submicron regime, device scaling is becoming increasingly difficult due to various physical and technological limitations. Furthermore, in a complementary metal-oxide-semiconductor (CMOS), technology hole mobility is lower than that of its electron counterpart. In order to match the current drives of n-channel metal-oxide-semiconductor (NMOS) and p-channel metal-oxide-semiconductor (PMOS) devices, the area of the PMOS device must be taken about two to three times larger than the NMOS device. This adversely affects the level of integration and device speed. In order to further improve the speed of VLSI circuits, however, new materials and device structures are being proposed. It has been shown recently that the in-plane electron mobility of a strained Si layer is significantly higher than that of bulk Si [1]–[4]. This concept has been used to fabricate high-performance NMOS devices on strained Si [5].

The prediction of higher hole [6] mobility in strained-Si has generated interest in the fabrication of strained-Si PMOSFET's. The fabrication of strained-Si PMOS has been demonstrated [7], and the experimental evidence of improved hole mobility in strained-Si PMOS has been provided [7]. Only limited data could be obtained from this PMOS because of the use of a poor process (subthreshold slope of 111 mV/decade and mobility of 94 $cm^2/V \cdot s$ for control Si device, 65 Å gate oxide allows gate bias of 0 to −2.0 V) and a 1 μm uniform-composition partially-relaxed SiGe buffer which is known to have a very high defect density [8]–[9]. Also, the mobility of the epitaxially grown strained-Si is compared with that of that of the bulk substrate which has different doping. In this work, we present in detail the growth of high-quality strained-Si layer using gas-source MBE. The strained-Si layer is characterized using photoluminescence (PL), X-ray diffraction, and transmission electron microscopy (TEM). We use an improved device structure and process to fabricate high-performance strained-Si PMOS: (1) high-quality (defect density $<10^5/cm^2$), step-graded, completely-relaxed thick (3 μm) SiGe buffer layer; (2) low thermal budget (maximum process temperature of 700 °C); (3) high-quality thick (100 Å) gate oxide (measurement presented from 0 to −5 V); (4) a control Si device with 5000 Å Si epi and the same doping as the strained-Si layer for device performance comparison; and (5) improved process (subthreshold slope of 82 mV/decade and mobility of 120 $cm^2/V \cdot s$ for Si device). In particular, this work presents for the first time the following experimental strained-Si PMOSFET results: (i) mobility of p-doped strained-Si layer; (ii) record high-field mobility improvement of 40% at 300 K and 200% at 77 K for strained-Si over bulk Si; (iii) Si/SiO_2 interface scattering found to be more severe for strained-Si layer, with high vertical-field (high $|V_g|$) data presented from 0 to −5 V; and (iv) demonstration of quantum confinement effect at the type-II strained-Si/SiGe-buffer interface using C-V measurements. This work clearly shows that the in-plane hole mobility of the strained-Si is higher than that of the bulk Si.

II. Device Structure

It has been recently shown that the in-plane hole mobility of strained-Si is higher than that of bulk Si [6]. With the application of uniaxial stress, the degeneracy between light and heavy hole bands in Si is lifted, thereby improving mobility through the reduction of interband scattering (Fig. 1). The in-plane hole mobility of low-doped strained-Si grown on $Si_{0.9}Ge_{0.1}$ is 2.4 times higher than that of low-doped bulk Si [6]. The strain in Si also splits the conduction band into 2-fold and 4-fold degenerate bands, resulting in a staggered type-

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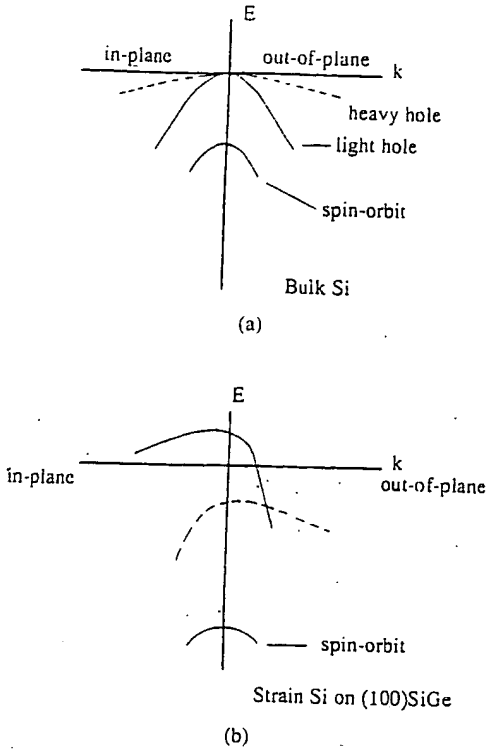


Fig. 1. Schematic diagram of the valence bands, (a) bulk Si, and (b) strained-Si layer on (100)SiGe substrate.

II band alignment in a relaxed-SiGe/strained-Si/relaxed-SiGe system (Fig. 2).

The strained-Si PMOSFET substrate consists of a Si(100), completely relaxed, graded SiGe buffer (3 μm) and epitaxially grown thin strained Si layer. The grading of Ge concentration in the SiGe buffer is essential in order to obtain a high-quality SiGe buffer layer [8]–[9]. A 100 Å gate oxide is thermally grown on strained-Si layer, thus forming a SiO_2/strained-Si/relaxed-SiGe MOS structure. For a Ge concentration of 18% in the buffer layer, the valence band offset at the strained-Si/SiGe-buffer interface is 120 mV, which is sufficient to confine holes in the strained-Si layer. The device operation can be understood by using an 1-D Poisson solver with appropriate band offsets. In this simulation, strained-Si thickness is taken as 150 Å and valence band offset is 150 meV. The substrate is n-type and the device uses a n^+ poly. At a low magnitude of gate voltage, the hole concentration in a PMOSFET at the strained-Si/SiGe-buffer interface can be higher than that at the SiO_2/strained-Si interface. In this case, the device behaves like a buried-channel device. The channel mobility of the device is primarily determined by the carrier scattering at the strained-Si/SiGe interface, with the scattering at the SiO_2/strained-Si diminished due to the larger distance between the interface and carriers (Fig. 3). However, when the magnitude of the gate voltage is increased further, the carriers at the SiO_2/strained-Si interface dominate channel conduction and the device behaves like a surface-channel device (Fig. 4). Under this condition, due to the higher mobility of strained-Si layer, the channel mobility of the strained-Si MOSFET is higher than that of the surface-channel bulk-Si device. It will be shown experimentally that under high vertical (high $|V_g|$) fields, the channel mobility of strained-Si device is considerably higher than that of the bulk-Si device.

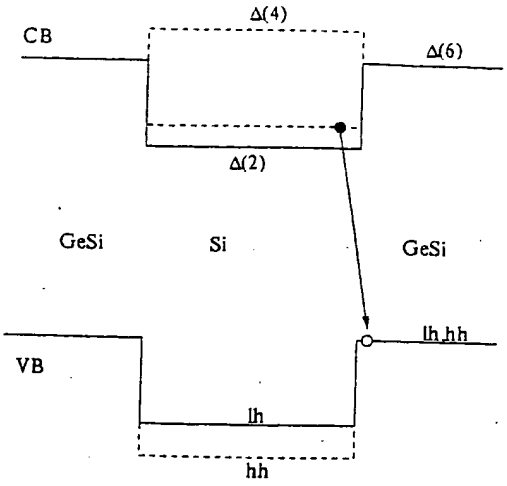


Fig. 2. Schematic diagram of the band alignment between relaxed-SiGe/strained-Si/relaxed-Si quantum well structure.

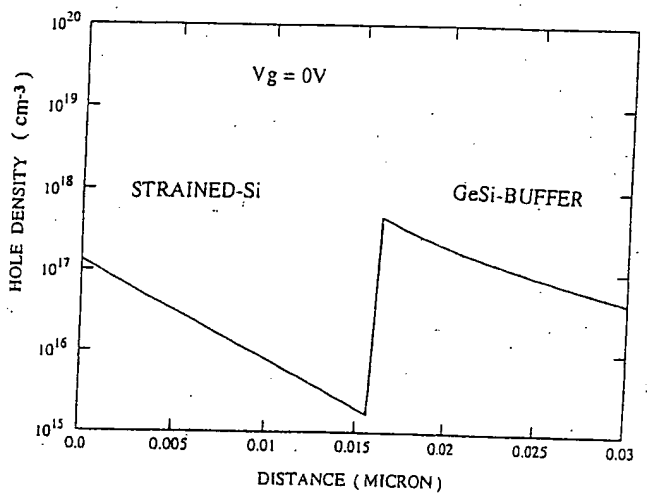


Fig. 3. Hole concentration as a function of distance from the SiO_2/strained-Si interface into the substrate in a SiO_2/strained-Si/SiGe-buffer MOS structure. The valence band offset between strained-Si/SiGe-buffer is assumed 150 eV in this simulation. The magnitude of gate bias is small ($V_g = 0$ V).

III. Growth of High Quality Strained-Si

The basic requirement for the growth of the strained-Si layer is to obtain a high-quality relaxed SiGe buffer layer on Si substrates. In this study, we use a step-graded buffer layer, which is grown by gas source MBE (Daido Sanso VCE-S2020) at 800 °C. The starting material consists of 3″, p-type, 5–10 Ω-cm, Si(100) wafer and 3000 Å Si buffer. The strain in Si (900 Å strained-Si on a 3 μm graded (0 to 18% Ge) SiGe buffer and a $Si_{0.82}Ge_{0.18}$ cap layer) is checked by double crystal X-ray diffraction (Fig. 5). A thicker strained Si layer is necessary to get good signal intensity from X-ray diffraction. Peak position of the X-ray signal from an epileyer with respect to peak position of the Si substrate is a measure of the out-of-plane lattice constant (perpendicular to the growth plane) of the epilayer. For graded SiGe buffer, the out-of-plane

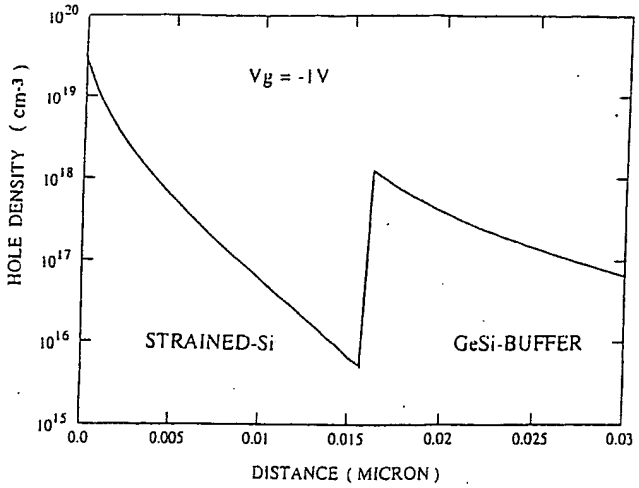


Fig. 4. Hole concentration as a function of distance from the SiO_2/strained-Si interface into the substrate in a SiO_2/strained-Si/SiGe-buffer MOS structure. The valence band offset between strained-Si/SiGe-buffer is assumed 150 eV in this simulation. The magnitude of gate bias ($V_g = -1$ V) is higher compared to Fig. 3.

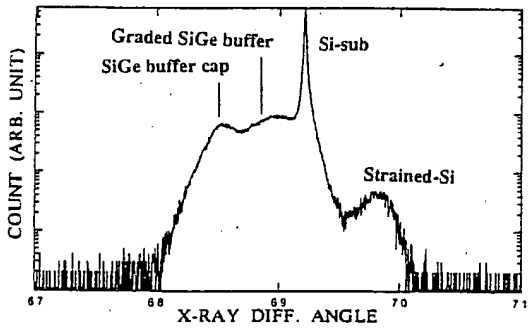
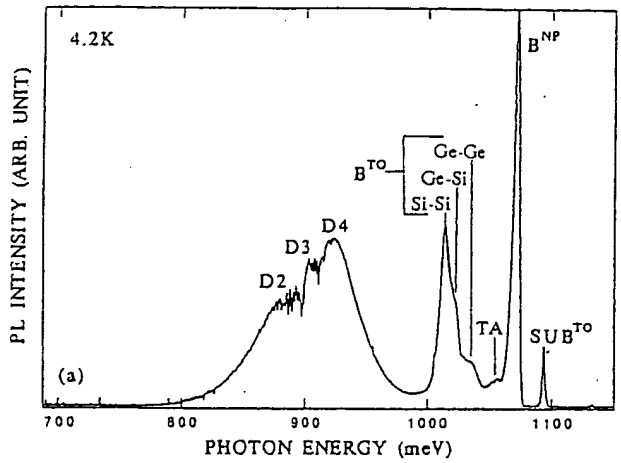
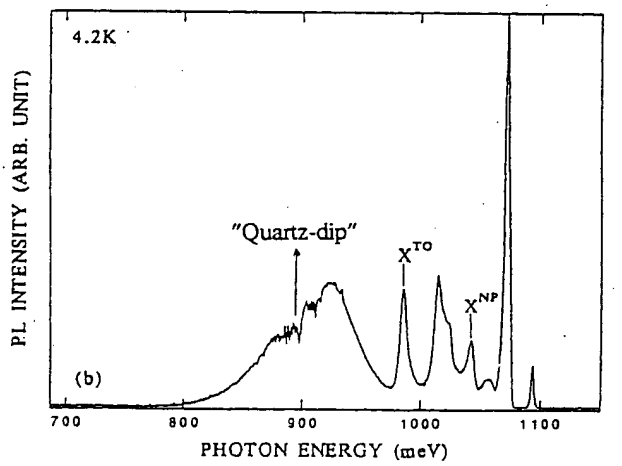


Fig. 5. The tensile strain in Si layer is demonstrated by double crystal X-ray diffraction. The strained-Si layer (900 Å) is grown on a 2.5 μm thick graded (0 to 18% Ge) SiGe buffer layer on (100)Si substrate.



(a)



(b)

Fig. 6. (a) Photoluminescence spectra at 4.2 K of a thick (6.3 μm), graded (0 to 18% Ge), and completely relaxed SiGe buffer layer. The sharp and large peak (B^{NP}) shows the high quality of the relaxed buffer. (b) PL spectra from the multiple strained-Si (18 Å) quantum wells (X^{TO} and X^{NP}) on this buffer.

lattice constant varies continuously with grading. Therefore, a broad peak appears to the left of substrate peak (Fig. 5). The left-most peak is the signal from the SiGe capping layer which contains 18% of Ge. Similar X-ray diffraction results were obtained for graded SiGe buffer using solid source MBE [12]. In contrary, when Si is grown epitaxially on SiGe buffer, which has higher in-plane (epi growth plane) lattice constant, the out-plane-plane lattice constant of strained-Si becomes smaller than that of bulk Si. This is because strained-Si experiences a tensile in-plane stress. This smaller lattice constant of strained-Si results in a X-ray peak right to the Si substrate peak. This is cearly demonstrated in Fig. 5.

Photoluminescence (PL) is a nondestructive method to study many optical and electronic properties of epitaxial layers. The full-width at half maximum (FWHM) of the no-phonon assisted optical transistion spectrum indicates the quality of the SiGe buffer layer. The presence of defects broadens the FWHM. In this study, PL is also used to determine band alignment between strained-Si and relaxed SiGe buffer as well as to determine band offsets at valence and conduction bands. In addition, we have used PL for the first time to study the strain and quality of the strained-Si layer. In the case of strained-Si quantum well, the excitonic optical transitions take place between the conduction band of strained-Si and the valence band of SiGe buffer (Fig. 2). These two regions are spatially separated. Furthermore, Si is an indirect bandgap material. These two factors reduces the probability of electronic transitions in strained Si layer. As shown in Fig. 6 below, a strong and clear signal from the strained-Si quantum well is a indication that good quality strain Si epitaxy has been achieved in this work. In order to study the type-II band alignment and the growth of the high-quality strained-Si layer using PL, five quantum wells with equal well width were grown on a thick (5 μm) buffer layer at 700 °C. The barrier between adjacent wells was 350 Å $Si_{0.82}Ge_{0.18}$, which eliminates any coupling between the quantum wells. All epitaxial layers were undoped. Fig. 6(a) shows PL spectra from a thick (6.3 μm), step-graded, relaxed $Ge_{0.18}Si_{0.82}$ buffer layer at 4.2 K. A peak at 1.093 eV, denoted as SUB^{TO}, is due to transverse-optical (TO) assisted excitonic recombination in Si substrate. A sharp peak at 1.072 eV corresponds to the no-phonon (NP) transition from the relaxed buffer layer.

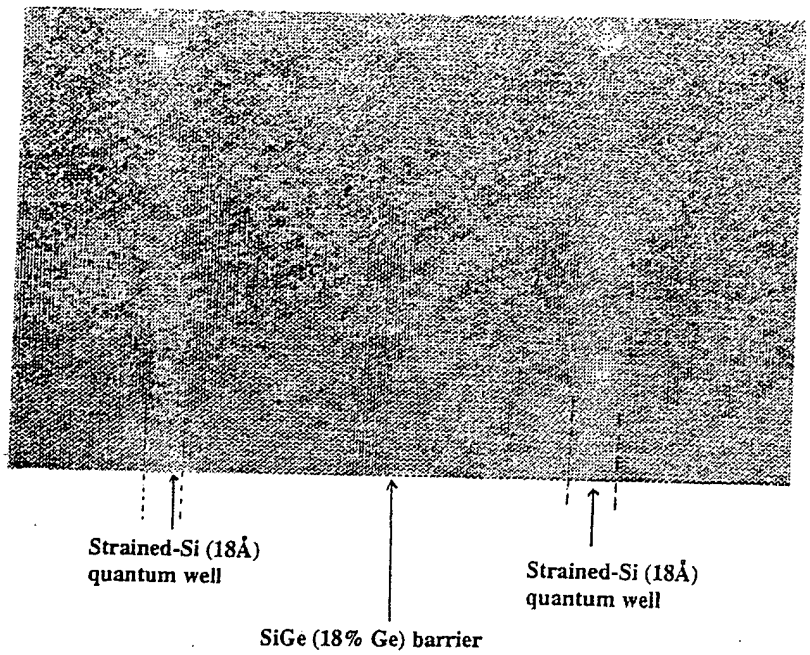


Fig. 7. Lattice image of the strained-Si layer (18 Å) grown on a step graded (0 to 18% Ge), relaxed SiGe buffer. Two quantum wells are shown in this figure.

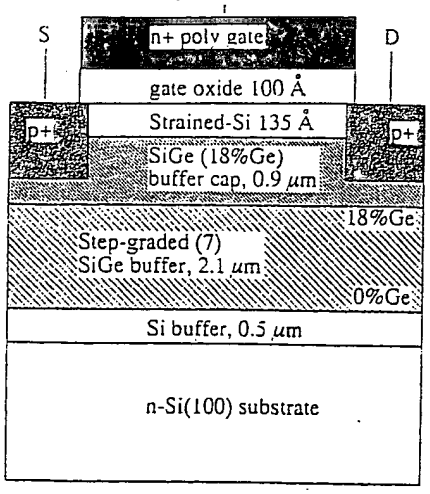
Transitions from the buffer (barrier) layer are denoted by "B." FWHM of this peak is 4.5 meV at 4.2 K, which shows that the top region of the buffer is of good quality. From FWHM study, the quality of the buffer layer is found to be comparable to that of the bulk SiGe alloy. For the bulk SiGe alloy, FWHM for 8% Ge is 15 meV and for 38% Ge is 6 meV [13]. For the solid source MBE grown sample (10% Ge/μm grading and 5 μm thick 30% Ge buffer cap layer), FWHM is 7 meV [14]. Phonon-assisted momentum-conserving transverse-acoustical (TA) and transverse-optical (TO) replicas are found at lower energies, TA at 16 meV, TO(Ge-Ge) at 36 meV, TO(Ge-Si) at 51 meV, and TO(Si-Si) at 58 meV. Broad peaks at 0.880, 0.906, and 0.923 eV are identified as dislocation- and point defect-related transitions D2, D3 and D4.

Five quantum wells with equal well width were grown on the above buffer layer at a lower temperature (700 °C) in order to avoid thermal relaxation of strain and Ge/Si interdiffusion in the quantum well. PL spectra from the multiple quantum wells are shown in Fig. 6(b). All transitions from the strained-Si quantum well are denoted by "×." Well and barrier widths were 10 Å and 350 Å, respectively. The PL spectrum in Fig. 6(b) looks identical to Fig. 6(a) except that two new peaks (as a pair) appear at 0.985 and 1.043 eV. We assign the peak at 0.985 eV to be the TO phonon-assisted band-edge transition of confined excitons in strained-Si quantum well. Therefore, the TO-assisted excitonic transition occurs between the confined conduction band state (lowest lying in energy) of the strained-Si quantum well and the top of the valence band of the SiGe buffer layer. The peak at 1.043 eV in Fig. 6(b) can be assigned to the NP transition from the quantum wells and always appears as a pair with the TO-assisted transition. These two peaks were separated by 58 meV, which corresponds to the TO phonon energy of Si-Si bond. The TEM lattice image of the quantum well (Fig. 7) shows the high quality of the strained-Si layer (18 Å). Two wells are shown in Fig. 7. The lattice image shows a smooth epitaxial interface between strained-Si and SiGe buffer without any lattice defects.

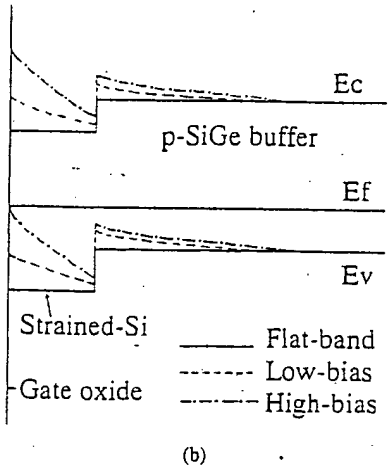
IV. Fabrication of Strained-Si PMOSFET

Fig. 8(a) shows the schematic diagram of the PMOS used in this study. The SiGe buffer and strained-Si layer are grown by gas source MBE at 800 and 700 °C, respectively. The PMOSFET's are fabricated using a standard self-aligned n^+-poly Si process. The devices were isolated with a 7000 Å LPCVD oxide. Strained-Si epilayer (180 Å) is thermally oxidized for 140 min at 700 °C to form a 100 Å gate oxide. Drain and source are implanted with 25 KeV boron at 6×10^{14} cm^{-2}. Drain/source implant activation is performed in two steps: (i) 550 °C for 100 min and (ii) 700 °C for 60 min in nitrogen. Low-temperature anneal helps in the solid phase epitaxial growth of damaged Si, whereas high temperature step helps in activating dopant atoms. Al is used as the contact metal, which is annealed in forming gas at 400 °C for 20 min. The maximum process temperature is maintained at 700 °C in order to avoid any devices degradation due to strain relaxation or interdiffusion. PMOSFET's are fabricated on two types of substrates. SUB-1 consists of a 0.5 μm Si epi layer (unintentionally doped p-type to 10^{16} cm^{-3}) on an n^- Si(100) substrate. SUB-2 consists of strained-Si on completely relaxed (verified by double-crystal X-ray diffraction) $Si_{0.82}Ge_{0.18}$ epi layers (unintentionally doped p-type to 10^{16} cm^{-3}) as shown in Fig. 8(a). Devices on SUB-1 and SUB-2 are depletion-mode devices due to the presence of p-type unintentional doping (Fig. 8(b)). The mobility improvement in the strained-Si layer is verified by comparing devices on SUB-1 and SUB-2.

Fig. 9 compares the measured capacitances of bulk-Si (SUB-1) and strained-Si (SUB-2) devices. The capacitance (Gate to Sub when Sub and S/D are tied together) was measured on a long-channel (W/L = 300 μm/100 μm) PMOSFET at 10 KHz. The plateau in the accumulation



(a)



(b)

Fig. 8. (a) Schematic diagram of a strained-Si PMOS, and (b) schematic band diagram in flat band and accumulation conditions.

capacitance clearly shows hole confinement at the strained-Si/SiGe-buffer interface at low magnitude of gate bias [10]. In particular, the C-V measurement provides the following results. (i) Thickness of thermally grown SiO_2 is 100 Å for both devices. This is also confirmed by ellipsometric measurements. (ii) Substrate doping for both devices is the same (10^{16} cm^{-3}). This is extracted from the minimum capacitance in the C-V curve. (iii) The experimental flatband voltage is -1.0 V for both devices. (iv) The plateau in the accumulation capacitance of the strained-Si device is due to the hole confinement at the strained-Si/SiGe-buffer interface. This occurs as the gate voltage (V_g) is swept from flatband to strong accumulation (-1 to -2 V). (v) In strong accumulation, the channel charge is dominated by the accumulation charge at the SiO_2/strained-Si interface and the charge at the strained-Si/SiGe-buffer can be neglected [11]. In strong accumulation ($V_g < -2$ V), therefore, strained-Si and bulk-Si devices are surface-channel devices and the effective gate oxide thickness for both devices is 100 Å of SiO_2. In this strong-accumulation regime, the accumulation charge in strained-Si and bulk-Si devices is the same (due to the same gate capacitance, same flatband voltage, and neglect of the charge at the strained-Si/SiGe-buffer interface). In fact, the maximum improvement

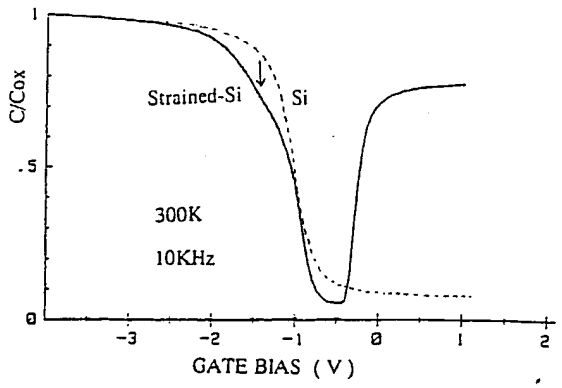
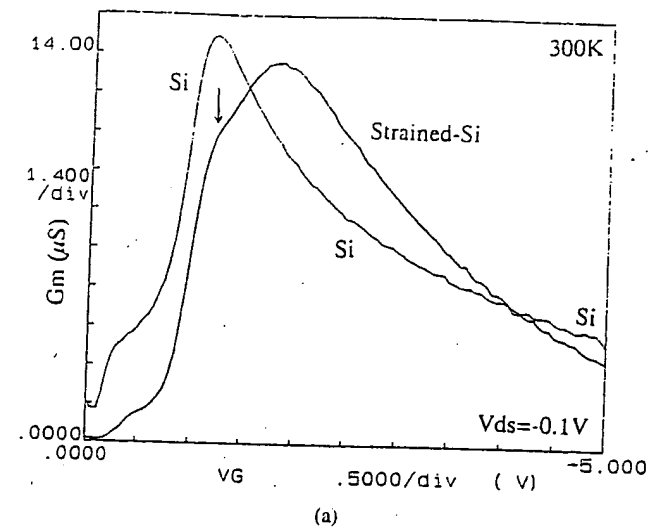


Fig. 9. Comparison of bulk-Si and strained-Si measured capacitances at 300 K. The capacitance was measured on a long-channel ($W/L = 300$ μm/100 μm) PMOSFET at 10 KHz.

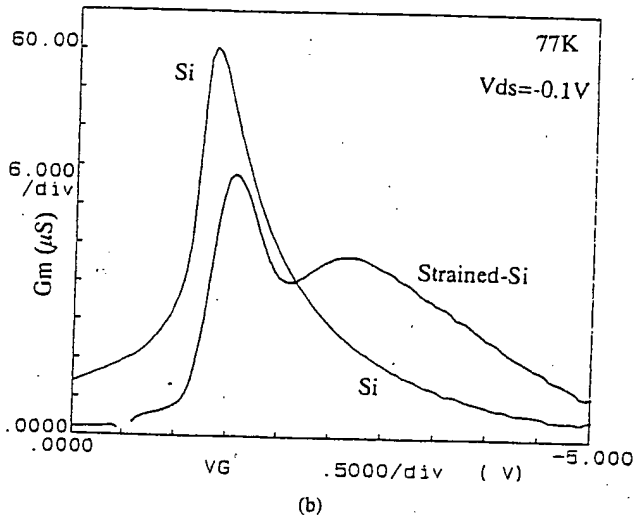
in mobility occurs in strong accumulation (-2.5 V and -4.0 V at 300 K and 77 K, respectively).

Only long-channel ($W/L = 300$ μm/100 μm) PMOSFET's are used for mobility comparison. The linear transconductances (G_m) of long-channel devices at 300 K are plotted in Fig. 10(a). As expected, the control Si device shows one large peak at -1.2 V. But strained-Si device G_m shows one shoulder at -1.25 V and one peak at -1.75 V at 300 K. The shoulder at -1.25 V (arrow) corresponds to hole confinement at the strained-Si/SiGe-buffer interface (see C-V results above). This is because at a low magnitude of gate bias (start of accumulation), the holes at the strained-Si/SiGe-buffer interface dominate channel conduction (Fig. 8(b)). In this low magnitude of gate bias, the effective gate oxide thickness is 145 Å (100 Å SiO_2 in series with 135 Å strained-Si layer) for the strained-Si device. Using this effective gate oxide thickness, the low-field channel mobilities for the strained-Si device are 190 and 570 $cm^2/V \cdot s$ at 300 K and 77 K, respectively. For the control Si device (gate oxide thickness 100 Å), low-field channel mobilities are found to be 140 and 580 $cm^2/V \cdot s$ at 300 K and 77 K, respectively. At higher magnitudes of gate voltage, however, the holes at the SiO_2/strained-Si interface dominate channel conduction (peak at -1.75 V) and the strained-Si device becomes a surface-channel device [11]. The transition from buried channel to surface channel is clearly seen at 77 K (peaks at -1.55 and -2.7 V) because hole confinement at the heterointerface becomes more pronounced at low temperature (low thermal energy of carriers (Fig. 10(b))).

For gate bias between -1.5 and -4 V, the strained-Si device shows higher mobility than that of the bulk-Si device (Fig. 11). The decrease of mobility with gate bias is more severe in the strained-Si device at 300 K and 77 K (Fig. 11). This fact is not understood. Surface roughness and quality of the strained-Si layer on SiGe buffer, which is known to have higher defect density and roughness compared to that of bulk Si substrate, may contribute to this difference in degradation mechanisms. Maximum improvement in high vertical (high $|Vg|$) field mobility for the strained-Si device is 40% at 300 K (effective gate oxide thickness for both devices is ٢٠٠ Å SiO_2). At 77 K, dramatic improvement of high-vertical (high $|V_g|$) field mobility is found for the strained-Si device for the

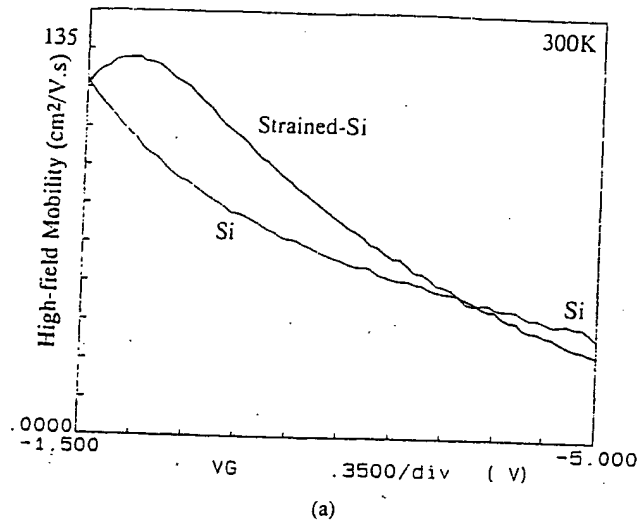


(a)

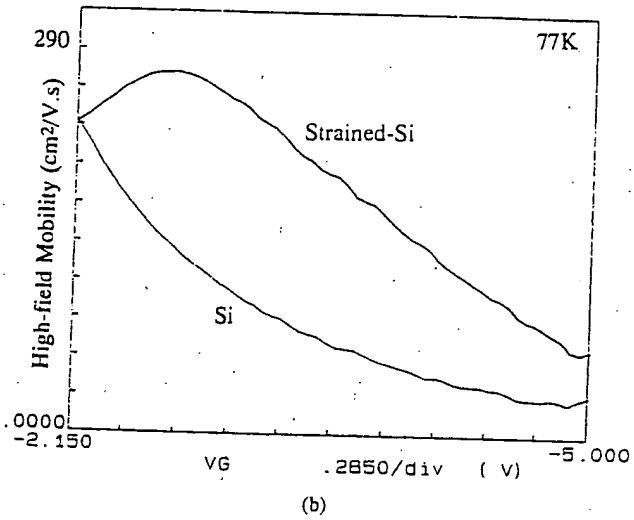


(b)

Fig. 10. Linear transconductances of long channel (W/L = 300 μm/100 μm) strained-Si and bulk Si PMOSFET's, (a) 300 K, and (b) 77 K.



(a)



(b)

Fig. 11. Comparison of mobilities at high vertical field (high $|V_g|$) at 300 K and 77 K. The y-axis label in this graph, "high-field", means highe vertical field (high $|V_g|$).

entire bias range of -1.5 to -5 V. The maximum mobility improvement of 200% at 77 K for strained-Si device is a record high (effective gate oxide thickness for both devices is 100 Å SiO_2). Although the accumulation-layer hole mobility is measured here, the inversion-layer mobility is known to be approximately the same as the accumulation-layer mobility in high fields [15]. This work clearly gives experimental evidence that the in-plane hole mobility of strained-Si is higher than that of bulk-Si [6].

I-V characteristics are given for strained-Si (Fig. 12), bulk Si with Si epi (Fig. 13), and bulk Si without any epi (Fig. 14) PMOSFET's. As explained earlier, unintentional boron doping in the epi layer makes it a depletion-mode device both for strained-Si and Si epi devices (Figs 12 and 13). Because of this, transistors do not turn off at $V_g = 0$ V. However, the channel mobility of these devices in accumulation can be compared, as described in [15]. At the higher magnitude of gate voltage, accumulation layer charge density increases at the surface and transistors show good saturation characteristics. The drain current at $V_g = 0$ V is due to the p-type doping of the epilayer and is not due to any other process problem.

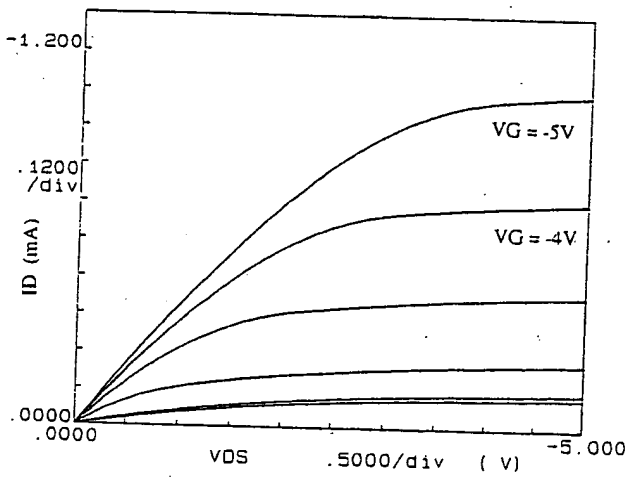


Fig. 12. I-V characteristics of long-channel (W/L = 300 μm/100 μm) strained-Si PMOSFET at 300 K. V_g step in -1 V.

This is confirmed by measuring the bulk Si (without any epi layer) MOSFET's. For the Si MOSFET without any epi layer, enhancement-mode device with good turn-on and turn-off

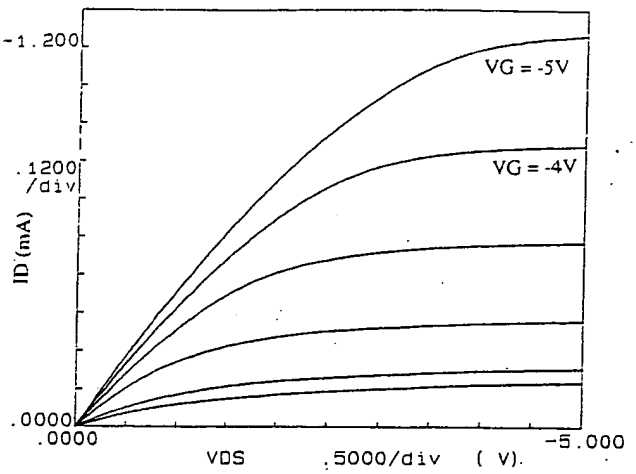


Fig. 13. I-V characteristics of long-channel (W/L = 300 μm/100 μm) bulk Si with Si epi PMOSFET at 300 K. V_g step in -1 V.

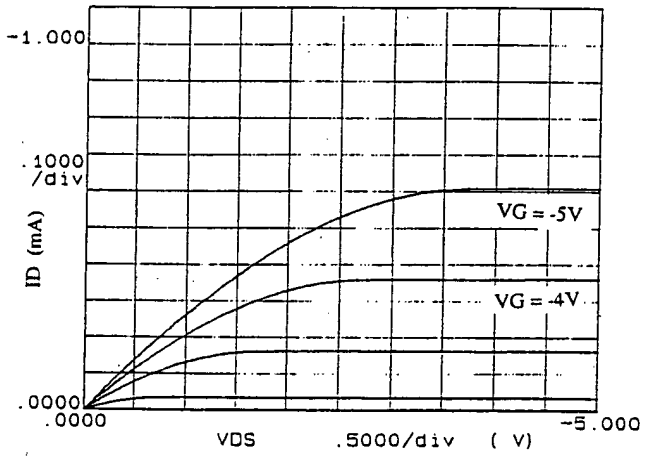


Fig. 14. I-V characteristics of long-channel (W/L = 300 μm/100 μm) bulk Si without any epi PMOSFET at 300 K. V_g step in -1 V.

characteristics is obtained as shown in Fig. 14 ($V_t = -1.29$ V, subthreshold slope 82 mV/decade).

V. Summary

In this work, the operation and fabrication of a new strained-Si PMOSFET were presented. The growth of high-quality strained-Si layer by gas-source MBE is confirmed by X-ray diffraction, PL, and TEM. The hole confinement at the type-II band structure has been demonstrated for the first time by C-V and device transconductance measurements. The channel mobility of this device at high vertical field (high $|V_g|$) is found to be 40% and 200% higher at 300 K and 77 K, respectively, than that of a similarly processed bulk Si PMOS. This work clearly demonstrates that biaxial tensile strain in Si improves the in-plane hole mobility over that of bulk Si.

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K. Goto, photograph and biography not available at the time of publication.

A. Yutani, photograph and biography not available at the time of publication.

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